Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **ENABLE A**
2. **A1**
3. **YB4**
4. **A2**
5. **YB3**
6. **A3**
7. **YB2**
8. **A4**
9. **YB1**
10. **GND**
11. **B1**
12. **YA4**
13. **B2**
14. **YA3**
15. **B3**
16. **YA2**
17. **B4**
18. **YA1**
19. **ENABLE B**
20. **VCC**

**.081”**

**.075”**

**12 11 10 9 8**

**18 19 20 1 2**

**13**

**14**

**15**

**16**

**17**

**7**

**6**

**5**

**4**

**3**

**MASK**

**REF**

**25HC244**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref: 25HC244**

**APPROVED BY: DK DIE SIZE .075” X .081” DATE: 8/17/21**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54HC244**

**DG 10.1.2**

#### Rev B, 7/1